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FUNCTIONAL VARIATION OF DUAL GATE MOS-JFET CCD TEST STRUCTURE"

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ABSTRACT

Drain voltages of a test structure of dual gate MOS-JFET CCD (TIJ J032) were measured by an advanced laser scanner. The potential variation of the test structure at various source and gate voltages were measured by monitoring drain voltages - with respect to the scanning laser position. In this repro% a fine continuous, constant energy He-Ne laser beam of the Multipurpose Microelectronic Advanced Laser Scanner (MMEALS) is utilized for the characterization of local variation of the sensor performance within the test structure. The characteristics were compared with whole device performance by the semiconductor parameter analyzer, The threshold gate voltage of the optimum device operation for a fixed source voltage was determined by monitoring drain voltages with respect to gate voltages while the laser illuminated on the device. Such threshold variables then were used to collect local responsivity of the test structure to find defects most vulnerable in design, fabrication and radiation, while the micron-size laser beam is scanning on the whole test structure in a controlled manner. Preliminary results show that excellent correlation between specifications characterized by the semiconductor parameter tester and those by lasers. Furthermore, the local variation of the drain voltages obtained by lasers closely reflects the details of the fabricated test structures. Thus, the new MMEALS could be used not oniy in testing design efficiency and performances but also in characterizing local variation of the device, which are vital for intelligent manufacturing of highly goal oriented microelectronic CCDS or active pixei sensors.

" The research described in this paper was carried out by the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics Space Administration under the NASA Microelectronic Space Radiation Effects Program.

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ABSTRACT

Drain voltages of a test structure of dual gate MOS-JFET CCD (TIJ J032) were measured by an advanced laser scanner. The potential variation of the test structure at various source and gate voltages were measured by monitoring drain voltages with respect to the scanning laser position. In this report, a fine continuous, constant energy He-Ne laser beam of the Multipurpose Microelectronic Advanced Laser Scanner (MMEAL S) is utilized for the characterization of local variation of the sensor performance within the test structure. The characteristics were compared with whole device performance by the semiconductor parameter analyzer. The threshold gate voltage of the optimum device operation for a fixed source voltage was determined by monitoring drain voltages with respect to gate voltages while the laser illuminated on the device. Such threshold variables then were used to collect local responsivity of the test structure to find defects most vulnerable in design, fabrication, and radiation, while the micron-size laser beam is scanning on the whole test structure in a controlled manner. Preliminary results show that excellent correlation between specifications characterized by the semiconductor parameter tester and those by lasers, Furthermore, the local variation of the drain voltages obtained by lasers closely reflects the details of the fabricated test structures. Thus, the new MMEALS could be used not only in testing design efficiency and performances, but also in characterizing local variation of the device, which are vital for intelligent manufacturing of highly goal oriented microelectronic CCDS or active pixel sensors.

1. INTRODUCTION

Laser scanning systems have been vigorously developed ever since a wide range of lasers have become available. However, utilization of the laser scanner in semiconductor devices has been limited to only a few areas such as solar cell modules [11 and cross sectional analysis of solid state multi-layer device materials. Recently, the technology for scanning, sensing, image processing, and laser manufacturing has become much more mature. opening up several new avenues of application. For example. the technology can now precisely locate a focused probing laser beam onto the exact position most vulnerable to damage at a fast (<one millisecond) rate [2], and automatically collect performance parameters from many points on the device thanks to easy access to personal computers. Various wavelength laser beam can be focused down to a 2 micron spot size, limited only by diffraction effects, making it possible to probe a specific layer of individual transistors. These technology advancements have made the Liner Scanner very attractive for utilization in nondestructive lateral and vertical characterization within an individual sensor pixel.

Microelectronic sensor devices employed in spacecraft applications are continuously exposed to the risk of energetic particles. If a cosmic ray or an energetic particle such as proton strike occurs. anomalies can range from a change in the analog state of the sensor to damage in the solid state semiconductor material. These cause changes in the device efficiency and possible permanent degradation to the device. In some cases, the device parameters (current and voltage) change only for a certain period after the radiation. To counter these problems, some manufacturers have evolved techniques to increase radiation resistance by hardening and by changing the integrated circuit and operational software designs. Testing of radiation sensitivity has, however, proven to be expensive and rime-consuming.

Charged particle interactions can also present severe problems to a solid state electronic system of CCDs in space due to the generation of soft and hard errors [3,4]. Proton environments of the space is a serious concern of space imaging projects. Energetic particle could generate damages in CCD and electron-hole pairs (3.6 eV/pair for silicon). Currently, a very large semiconductor integrated parametric test system is required to assess the overall functional sensitivity of CCDs to proton radiation. Radiation hardness verification testing of design changes, or effectiveness of radiation hardening in

packaged devices is expensive and time consuming. These tests can also be performed with photons (light) having an energy larger than the semiconductor bandgap (1.1 eV for silicon), because they produce electron-hole pairs in the device as inject parametric testers (for example, HP4145). In addition, a laser beam can locally (both in vertical and horizontal) produce enough free carriers (6. lx 10^{26} pairs/cm^3 for 1 mW He-Ne laser) to characterize integrated circuits without the attendant difficulties of other techniques, and is quite economical. Accessibility to any single component in a circuit makes it suitable for routine testing of circuits for defect sensitivity, such as pixel cross talks.

Virtual phase technology is a well known technology for fabrication of lwgc-area CCDs. Correct information of the gate oxide surface potential pinned to the substrate potential and of the maximum buried channel potential are essential for a high charge transfer efficiency in bulk channel CCDs [5, 6]. The actual device performance parameters, such as necessary gate potentials, and clock swing for the optimum device operation should be determined. By changing gate bias for each fixed source voltage, the built-in potential margin as well as the clock well potential collapse are directly observable by this technology.

In this report, potential variation within the clocked well-virtual barrier (CWVB) and clocked barrier-virluai well (CBVW) of the duai gate MOS-JFET CCD test structures (TIJ J032) were measured as a function of gate bias voltage at a fixed source voltage under the local irradiation of the He-Ne laser. Since the drain voltage of a test structure at a fixed source voltages depends upon charges collected at the drain, the voltage variation of a drain at a fixed gate voltage depends upon the profile of the fabricated buried channel CCD and the physical defects of the structure when the laser power is constant. The potential in a buried channel silicon CCD test structure was also characterized after an irradiation of 250 Krad of 250KeV protons(10^{12} protons/cm^2) at room temperature to see the nature of tile defects due to the proton radiation. For the quality assurance of the device reliability against potential operational failures, preliminary test results were aiso discussed comparing with the total device performance collected by parameter tester to understand the physical and functional optimization of the devices.

2. TEST STRUCTURES

Figure 1 shows the overall optical view of the device, while Figure 2 shows the dual gate MOS JFET test transistors. Five aluminum wires were bonded to the pads of bulk(l)), source(S), gate(G), drain 1 (D 1) and drain 2(D2) and to respective posts for these measurements. Close-up SEM views of the test structures (CWVB and CBVW) are also shown in Figure 3. These transistors correspond to the virtual well-clocked barrier and clocked well-virtual barrier regions in the virtual phase CCD, and are fabricated at the same time as the virtual phase CCD imager. These transistors are used to measure the potential energy of barriers and wells, as affected by the variations of the gate bias. Using these devices the clocked well potential collapse as well as the built-in potential margin necessary to develop lateral fringing fields arc directly observed. In addition, values for potential well levels and the necessary clock swing for proper device operation arc easily

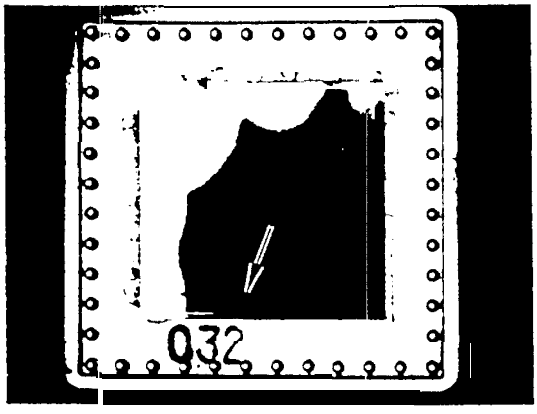


Figure 1. Overall optical view of the device, TIJ J032. Arrow indicates the test structures.

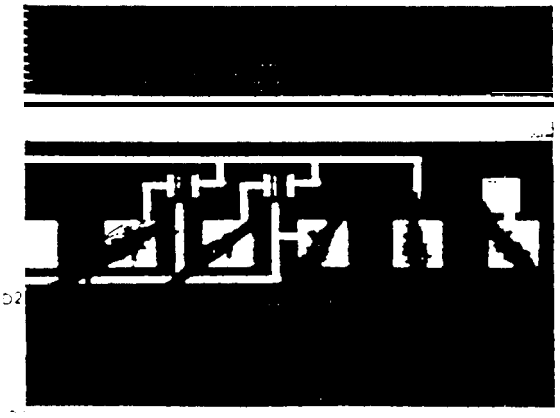


Figure 2. Close-up view of the test structures, Five wire bondings were made for these tests. B: Bulk, S: Source, G: Gate, D1: Drain of CWVB, and D2 : Drain of CBVW.

determined. These devices, therefore. serve as efficient process monitoring tools.

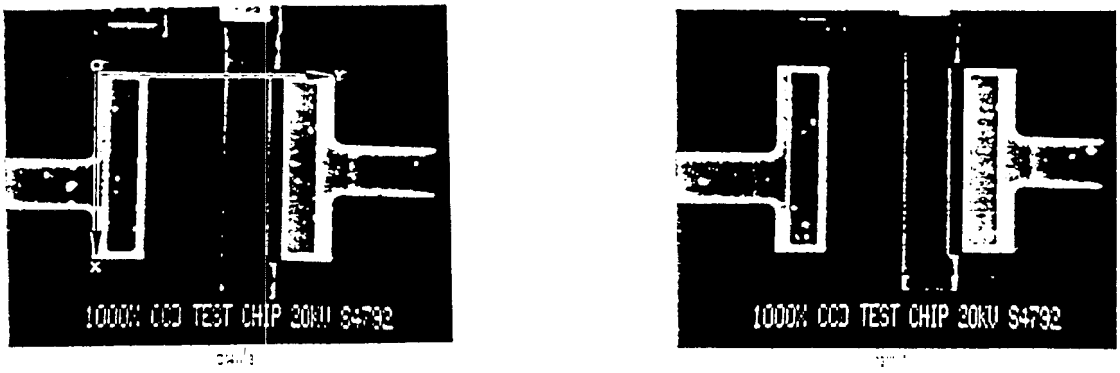


Figure 3. SEM views of the test structure. CWVB, CBVW. The arrows indicate the areas scanned by the advanced laser scanner for the drain potential variation.

A cross section of a two-phase CCD along the charge transfer channel is shown in Figure 4. In this design, charge transfer directionality is achieved by placing suitable implants under various portions of the phase electrodes, as indicated by "+" or "-" signs. These implants produce permanent potential barriers and wells which are raised and lowered by application of the appropriate voltages on the overlying gates to provide complete and unidirectional charge transfer. In virtual phase device, the electrode which is maintained at the dc potential is not built above the gate dielectric as a separate structure, but rather is built directly into the silicon surface and is biased at the substrate potential.

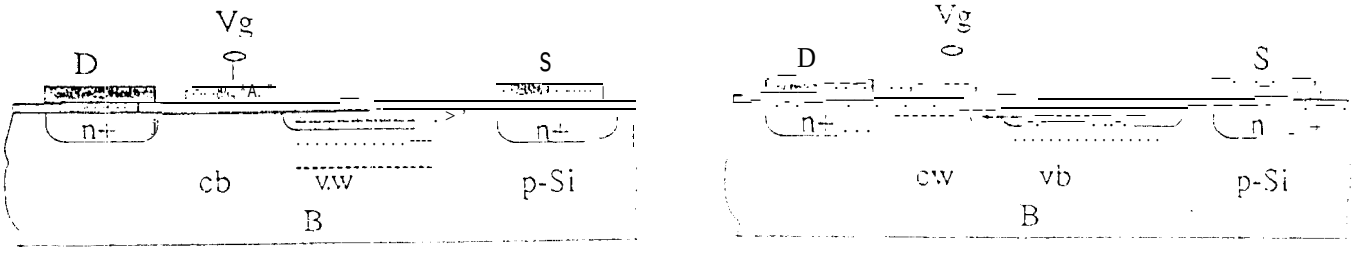


Figure 4. Schematic cross section diagram of the test structures

one important feature of the buried channel structure to note is that electrons are stored away from the surface. Therefore, free from the undesirable influence of surface scattering and traps. Another important feature of the buried channel structure is called the potential pinning phenomena. As the gate potential V_G is lowered toward more negative bias, the surface potential V_s also is lowered until it reaches the point where $V_s = 0$. When this occurs, the holes from the channel stops will flow across the surface and prevent further lowering of V_s. Therefore, V_s is pinned to zero. Since the holes can occupy only a very thin region of space near the surface of the silicon. the potential profile within the silicon will not be affected by the number of holes needed to compensate any additional field induced by the gate. As a result, the maximum value of V_G also will be pinned to some value, regardless of further lowering of the gate potential. Since the pinned potential profile of the buried channel structure, signal charge (electrons) can be effectively stored or transferred under the accumulated layer of holes, independent of further changes of the voltage on the overlying gate. in this case the holes accumulated at the surface act as a virtual gate for the underlying buried channel region.

3. LASER SCANNER TEST

The multipurpose microelectronic advanced laser scanner (MMEAL.S), as shown in Figure 5, is based on the principle that photons that have energies greater than the gap of the semiconductor can be absorbed. producing electron/hole pairs in the device under test. In the MMEAL.S, light from a continuous He-Ne laser beam is focused at selected locations on an

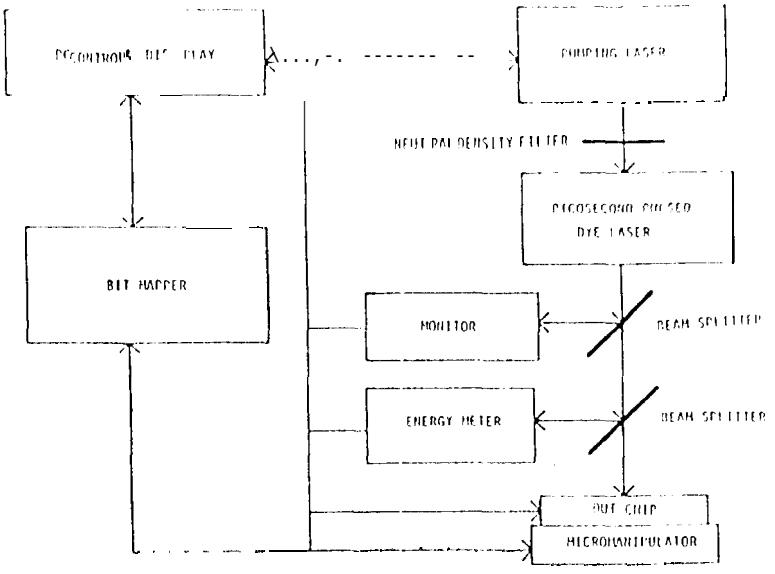


Figure 5. Test setup of the MMEALS.

integrated circuit to test for vulnerability of those locations to device performance. The beam can be scanned from one location to another in a controlled manner to identify sensitive areas. The wavelength and energy of the laser beam can be tuned to vary the effective depth of penetration of the photons so as to probe the layers of the circuit with great sensitivity. It is an opto/electro/mechanical apparatus for nondestructive testing of integrated sensors, logic circuits, and other microelectronic devices. MMEALS is in addition, a multipurpose diagnostic system that can be used to determine ultrafast time response, leakage, and electrical overstress in complex ICs utilizing other device information such as mask patterns and device parameters. Most notably, it can be used to simulate the effects of heavy ions accelerated to high energies and then determine the susceptibility of a digital device to single-event upsets (changes in stored bits unaccompanied by significant permanent damage) as well as latchups[2].

By slowly scanning the laser beam on the microelectronic components in an integrated circuit, the most sensitive component of the integrated circuits can be identified and plotted on an optical bit map of the device. Such variables as the laser energy deposited in the device under test, and the threshold value causing faulty performance can be plotted, and use to explore methods to optimized the device performance [7].

Because of fundamental differences between irradiation by laser at an isolated portion of an electric component and injecting carriers in to the device by electrically biasing the device, caution must be exercised in interpreting the results of tests on the MMEALS. For example. one difference is that the track of electron/hole pairs injected by a semiconductor parameter analyzer reflects the whole device performance, while that of the carriers generated by laser beam irradiated on a component represents only the performance of a local part of the integrated device. Another difference is that the density of charge earners produced by the laser beam decreases approximately exponentially with depth of penetration, while that of an injected carrier does not. Still other differences involve energies and mechanism of interaction wrth the semiconductor structure and distributions of charge carriers. Despite these differences, initial results show excellent agreement between parts characterized by laser and parametric analyzer. Thus the new MMEAI ,S represents both an efficient way of characterizing parts and, for the first time, identifying key elements of concern in a given device local structure.

4. POTENTIAL DISTRIBUTION OF THE TEST STRUCTURES

The drain voltage of the test structures (CBVW and CWVB) 01 the dual gate MOS-JFET CCD (TIJ J032) were measured both by a parametric tester and MMEALS. The details of the parametric lest condition of 111'4145 were shown in Table I

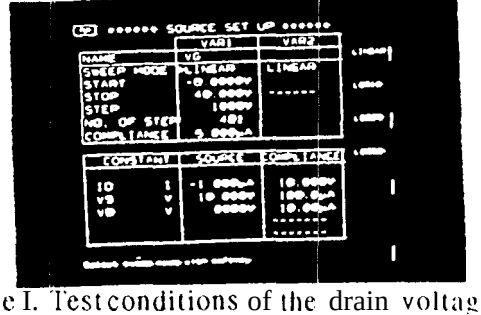
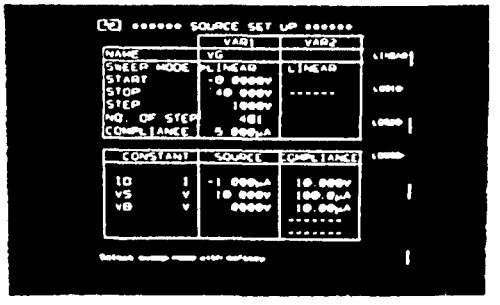


Table I. Test conditions of the drain voltages of CBVW vs gale Voltages.



'1'able II. Test conditions of the drain voltages of CWVB vs gate voltages.

and II. The gate voltages were changed over the range from -8.0 volts to + 40 volts. The voltages of the drain at several fixed gate voltages under a source voltage of 10 volts were monitored by scanning a focused He-Ne laser (wavelength: 632.8 nanometer) beam over the test transistors. The beam diameter of the laser is about 2 microns and the power of the laser is one microwatt.

Figures 6 and 7 show the drain voltage variation of the CBVW at 10 volts of source voltage with respect to various gate voltages by HP4145 parameter tester and by MMEAL S. For the both measurements, the clocked barrier were pinned at V_G = - 5.5 volts to V_D = 2.0 volts, while the V_D saturated to 4.4 volts at V_G = - 3.0 volts. This indicates that the gate voltage should be regulated by the system clock for the needed potential barrier shift from lower than - 5.5 volts to higher than -3.0 volts for the effective charge transfer for this device.

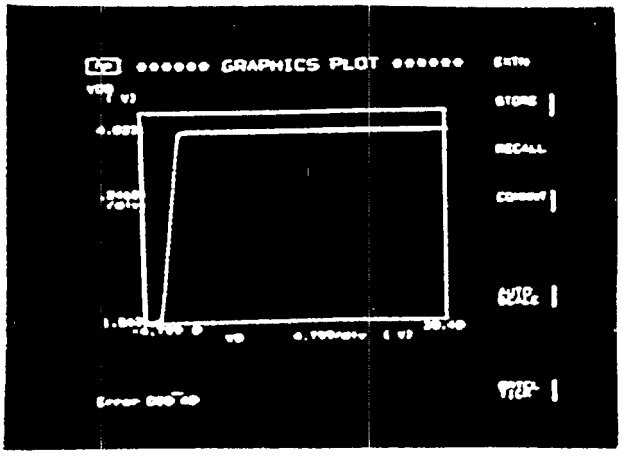


Figure 6. Change of the drain voltage of CBVW with respect to gate voltage under He-Ne laser irradiation by HP4145.

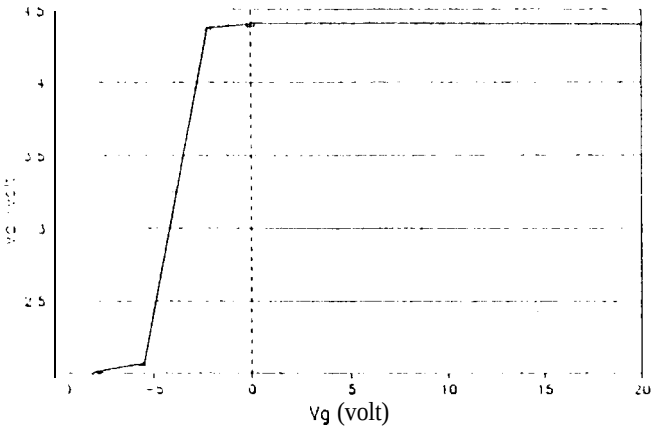


Figure 7. Discrete measurements of the change of drain voltage, V_D, of CBVW with respect to gate voltage, V_G, under He-Ne laser irradiation.

Similar results for the test structure of CWVB are shown in Figures 8 and 9. V_D were pinned to be 2.1 volts at V_G = -6.0 volts and V_D were saturated at 2.7 volts when V_G = -4.0 volts for both HP4145 and MMEAL S tests.

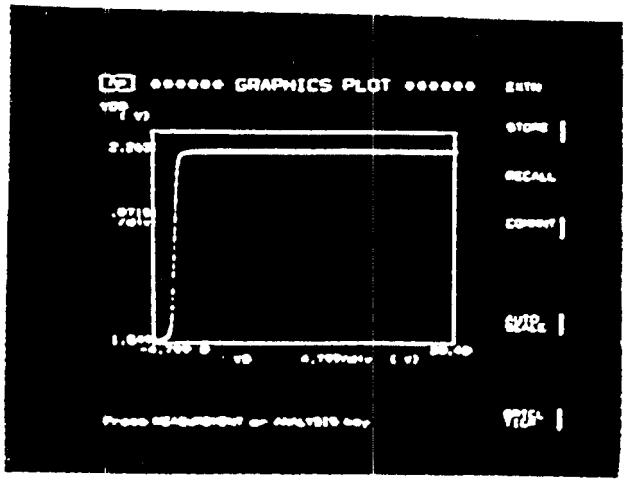


Figure 8. Change of the drain voltage of CWVB with respect to gate voltage under He-Ne laser irradiation by HP4145.

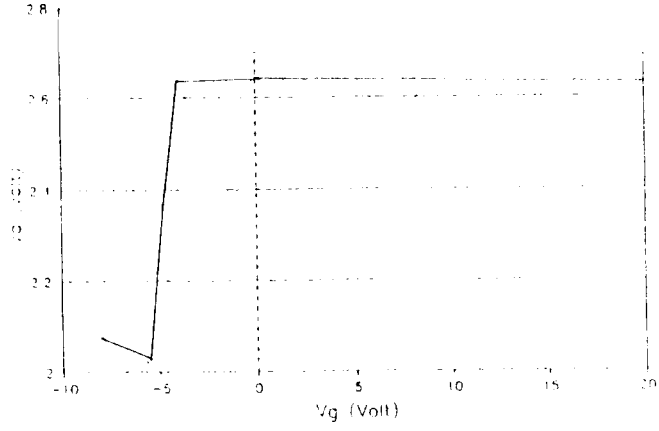
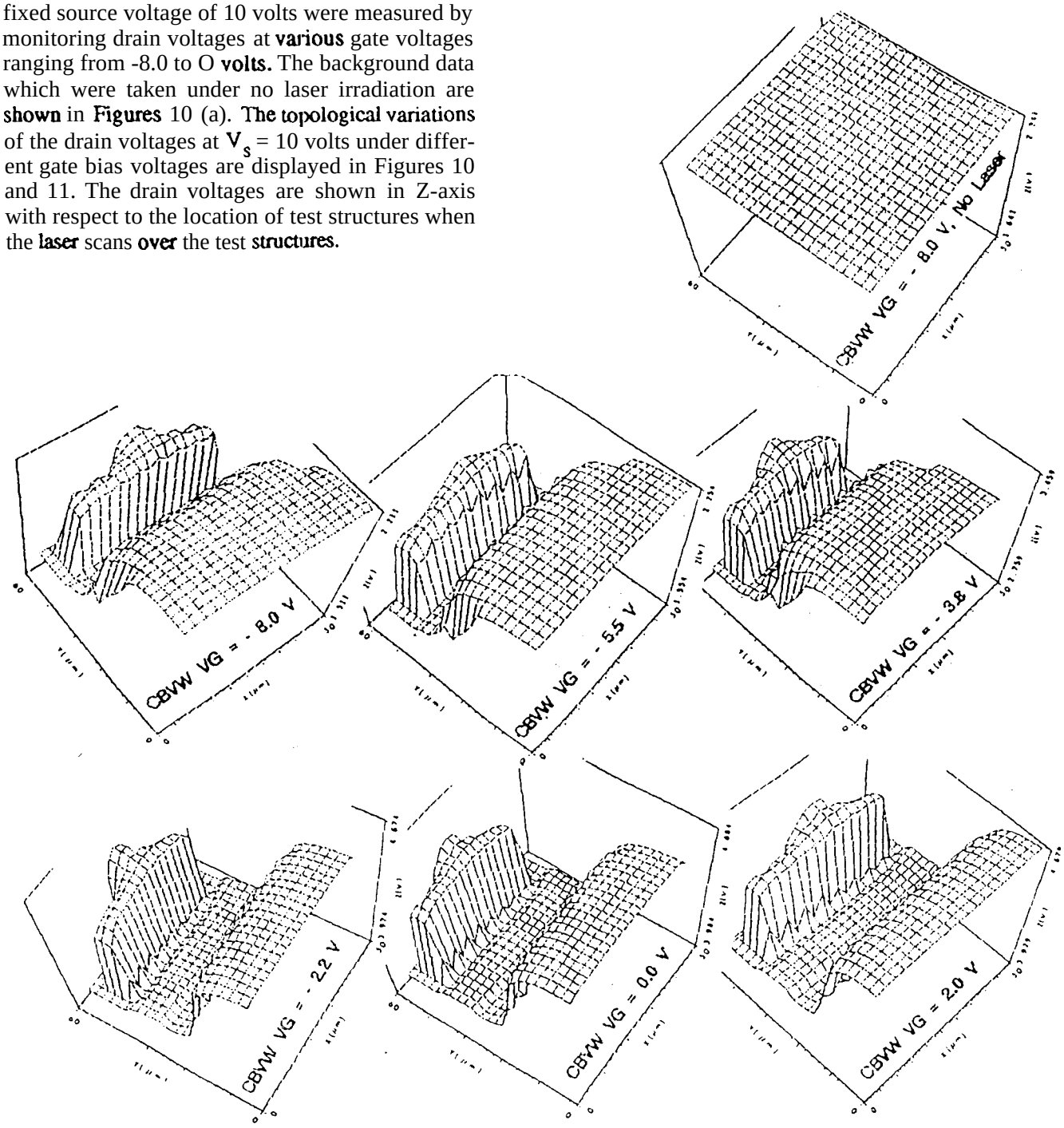
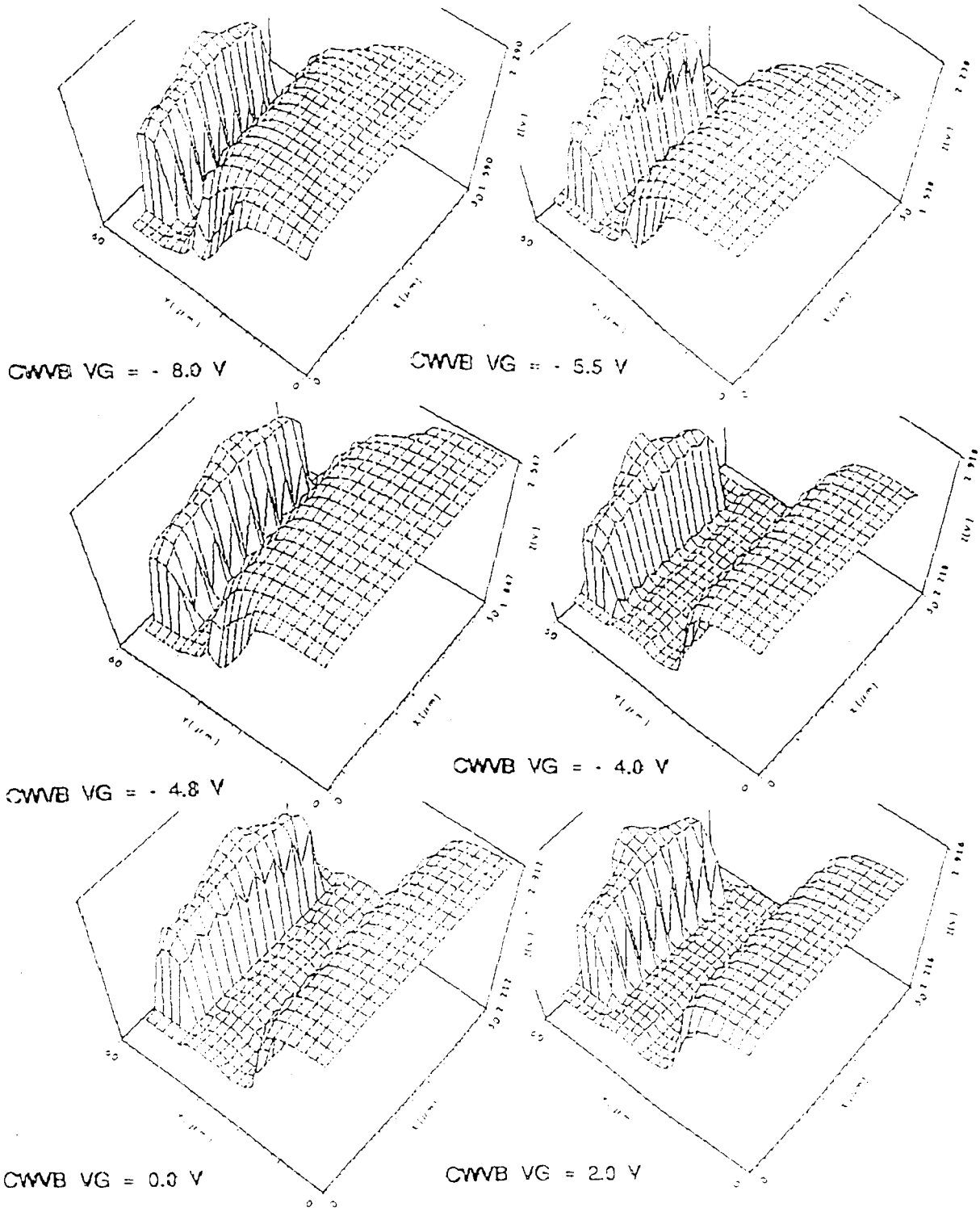


Figure 9. Discrete measurements of the change of drain voltage, V_D, of CWVB with respect to gate voltage, V_G, under He-Ne laser irradiation.

The potential distribution of the test structures at a fixed source voltage of 10 volts were measured by monitoring drain voltages at various gate voltages ranging from -8.0 to O volts. The background data which were taken under no laser irradiation are shown in Figures 10 (a). The topological variations of the drain voltages at V_s = 10 volts under different gate bias voltages are displayed in Figures 10 and 11. The drain voltages are shown in Z-axis with respect to the location of test structures when the laser scans over the test structures.



Figures 10 (a)-(g). Topological displays of the drain voltage at several different gate bias voltages for the test structure CBVW.



Figures 11 (a)-(g). Topological displays of the drain voltage at several different gate bias voltages for the test structure CWVB.

Note that the scales of Z-variables of all plots are the same (700 mV) for a direct visual comparison, but the ranges of the Z-axes are shifted according to the average drain voltages. The measured drain voltages were shown in Z-axis with respect to the area (X x Y = 50 μm x 60 μm) scanned by the liner. Any sudden deviation from the average drain potential can be interpreted as physical defects of a device. No deviations *were* found in this test. Had there been such deviation, however, the nature of the defects could be analyzed using these test results as a guideline by further destructive analysis. This information could then be utilized for screening high reliability imaging systems for space application.

Note also that the *clocked barrier* collapsed at V_G became higher than -3.8 volts for the CBVW as shown in Figure 10 (d). while the clocked well were collapsed when the gate voltage became higher than -4.8 volts for the CWVB as can be seen in Figure 11 (c). This means that the MMEAL.S can use not only for an optimizing tire device parameters but also for the efficient process manufacturing tool of the CCD fabrication.

5. EFFECTS OF THE PROTON DAMAGE

Two general types of CCD radiation damage important to the CCD have been previously reported as ionization and bulk damage. Recent analytical and experimental work has provided new insights into the production of damage sites in silicon CCDS by energetic particles[2]. In order to examine the change of the potential structure, the test structures were irradiated by protons at room temperature (10^{12} protons at a flux of 1x108 protons/see. cm^2). In this experiment, the protons are approximately monoenergetic at 250 KeV. The darnaged test structure was then characterized using both MEAI .S and the parametric tester. The clocked well was collapsed as usual when the gate voltage was lower down by about 1.0 volt which is the same as before radiation as shown in Figures 10 (d) and 11 (c). Bulk damage could be induced in the silicon material on which the device is fabricated. Bulk damage occurs when radiation events displace silicon atoms in the lattice structure creating bulk traps. In addition, electrons from the silicon valence band can thermally hop to trapping centers generating high dark current and creating hot pixels or dark spikes. However, no significant shifts of the gate voltages between the pinning and saturation voltages were observed 17 days after the radiation as shown in Table III. This is probably because of the radiation was performed at room temperature.

Table HI. *Change* of the gate voltage difference% between pinning and saturation after the proton irradiation.

Annealing time(Hrs)	o	12	139	374	422
Shifts(Volts)	1.11	1.20	1.07	1.06	1.00

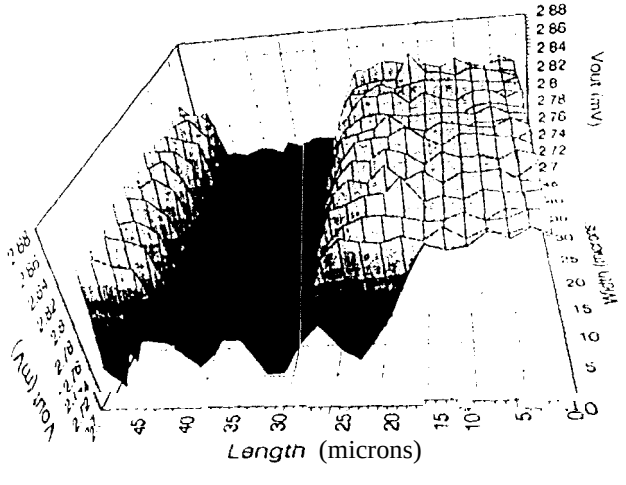


Figure 12 shows the variation of the drain voltage (V_D) of CWVB with respect to gate voltage (V_G) after the proton irradiation. The depth of the clocked well at the same gate voltage of - 4.0 Volts was reduced to 29% (0.2 Volts) from the initial potential depth of 0.7 volts. When electron-hole pairs are generated by energetic p.articles passing through the insulator of the gate oxide, ionizing damage arises. The charge created can be trapped in the insulator resulting in flat-band shift in the clock operating voltages to the CCD resulting degradation of the charge transfer efficiency (CTE). Charges buildup in the oxide become trapped at the gate $Si\text{-}SiO_2$ interface [3]. These results may reflect the degradationot the potential profile of the test structure after the proton irradiation regardless of their origins.

Figure 12. Topological map of the potential distribution of the CWVB after 10^{12} proton irradiation at room temperature. The device were functioning properly even after the proton irradiation. However, the built-in potential of the test structure were degraded to 29% as shown in Table IV.

Table IV shows that shifts of the threshold voltage of the test structure after the proton irradiation at room temperature. Initial increase of the threshold voltage followed by the decrease below than the initial voltage has been observed as was reported elsewhere. Further anal ysis is on the way for the performance related to this observations.

Table IV. Change of the Built-in potential depth with a the test structure CWVB after the proton irradiation.

Annealing Time(h)	0	1.6	21	120	422
Depth(volts)	0.72	0.16	0.14	0.14	0.14

6. CONCLUSIONS

In the Multipurpose Microelectronic Advanced Laser Scanner (MMEALS), light from a focused, continuous laser beam is utilized. The laser beam is scanned in a controlled manner to characterize the efficiency of the device performance within the test structures, and then precisely focused on selected locations to test individual IC *elements. Laser* energy, wavelength, pulse duration, etc. can be varied in order to determine the threshold value, depth, and location of the most sensitive regions on the IC. Initial results of the local functional response of the test structures shows excellent agreement with those of the parametric tester. Thus, the new mMEALS represents both an efficient and inexpensive way of characterizing CCDs.

7. ACKNOWLEDGMENTS

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References herein to any specific commercial product, process, or service by trade name, trade mark, manufacturer, or otherwise does not constitute or imply its endorsement by the United State Government or the Jet propulsion Laboratory, California Institute of Technology.

8. REFERENCES

[1]. K. Lehovec and A. Fedetowsky, " Scanning light spot analysis of faulty solar cells", Solid State Electron., 23, p.365, 1980.

[2]. Q. Kim, H. R. Schwartz, L. D. Edmonds and J. A. Zoutendyk, " Diagnosis of NMOS DRAM Functional Performance as Affected by a Picosecond dyc Laser", Solid-State Electronics, Vol. 35, No. 7, p.905, 1992

[3]. J. Janesick, G. Soli, T. Elliot, and S. Collins, "The Effects of Proton Damage on Charge-Coupled Devices", Proc. SPIE vol 1447, pp 87-108, 1990.

[4]. A. Simone, 1. Defusschere, A. Alderts, and C. Claeeys, "Ionozing radiation hardening of CCD Technology", IEEE, Trans. NS-39, p. 1964, 1992.

[5]. J. Hynecek, IEEE Trans. Electron Devices, ED-28, 483, 1981.

[6]. J. Janesick, T. Elliot, A. Dingizian, R. Bredthauer, C. Chandler, J. Westhpal, and J. Gunn, "New Advancements in Charge-Coupled Device Technology - Sub-electron Noise and 4096x4096 Pixel CCDs", CCDs in Astronomy, Astronomy Society of the Pacific, Vol.8 , Ed. G. Jacoby, 1989.

[7]. S. Mendis, S. E. Kemeny, R. C. Gee, B. Pain, Q. Kim. and F. R., Fossum, "Progress in CMOS Active Pixel Image Sensor", Proceed. SPIE Vol. 2172, Charge-Coupled Devices and Solid State Optical Sensors IV, 1994.